The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 13

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TINKU ACHARYA

Appeal No. 2004-0124
Application No. 09/432,337

ON BRIEF

Before HAIRSTON, GROSS, and BLANKENSHIP, Administrative Patent Judges.

BLANKENSHIP, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-3 and 9-11.

We reverse.

BACKGROUND

The invention is directed to a digital filter that includes a processing chain that has a selectable number of taps. Claim 1 is reproduced below.

1. A digital signal processing circuit comprising:

a chain of processing units to receive indications of discrete input values, each processing unit being associated with one of a group of filter coefficients; and

a tap selection circuit to select a group of the processing units of the chain to produce an indication of a filtered discrete output value for each discrete input value.

The examiner relies on the following reference:

Lesthievent et al. (Lesthievent)	6,125,155	Sep. 26, 2000 (filed Oct. 18, 1996)

Claims 1-3 and 9-11 stand rejected under 35 U.S.C. § 103 as being unpatentable over Lesthievent.

Claims 4-8 are objected to, but allowable if rewritten in independent form.

We refer to the Final Rejection (Paper No. 6) and the Examiner's Answer (Paper No. 11) for a statement of the examiner's position and to the Brief (Paper No. 10) for appellant's position with respect to the claims which stand rejected.

OPINION

The examiner finds that Lesthievent discloses, in Figure 4, a filter architecture having Q physical stages, which are considered to correspond to the claimed "chain of

processing units." The switches which are capable of connecting the input and the delayed inputs to corresponding multipliers for producing an output are deemed to be capable of providing the "the equivalent function" to the claimed "tap selection circuit." The rejection concludes, with respect to sole independent claim 1 on appeal, that it would have been obvious "to design the claimed invention" according to the teachings of the reference, because "the reference is a digital filter having selecting features as claimed." (Answer at 3.) Appellant, in the Brief, contends that Lesthievent fails to teach or suggest a tap selection circuit. The examiner adds, in response, that the delay "z" as described in the reference is an "interchanged term" for "tap" in the filter art. Thus, the delays "z" and switches are capable of "performing the equivalent function" of the tap selection circuit to select a group of processing units. (Answer at 5.)

Lesthievent describes, at column 2, line 44 et seq., a prior art digital filter over which the disclosed invention of the reference is to be an improvement. The filter architecture comprises Q physical stages with the input data x(n) shared over all of the stages by means of shift registers, and with the Q stages being summed to restore the filtered signal y(n) at the output O. The input data x(n) presented to the input of each stage is selected by means of a number (Q) of switches, which are activated at the output frequency rate Fs. The selected samples are then multiplied by the filter coefficients.

We agree with appellant that the rejection fails to set forth a case for prima facie unpatentability of the claimed invention. The examiner has not provided evidence or

explanation as to why the filter architecture of Figure 4 of the reference may be considered a "chain" of processing units. Each stage, as shown in Figure 4, appears to have as an input only the input signal x(n), or a delayed version of the input signal; i.e., the stages are substantially in parallel, receiving only present or delayed versions of the input signal. The examiner has not provided evidence or explanation as to how the sample-and-hold mechanism of the reference may be "equivalent" to the tap selection circuit as disclosed or claimed, nor, for that matter, why the "equivalence" would have been recognized by the artisan. The reference does not clearly disclose the capability of selecting a subset of the switches shown, as the rejection seems to suggest, but appears to describe all the switches being actuated at the output frequency rate; i.e., for the "useful samples" retained at the output. Finally, even if "delay," or "z," and "tap" are synonymous terms -- the examiner has pointed to no evidence in this record in support of the assertion -- it is unclear how Lesthievent may be deemed to disclose "delay selection" or "z selection" circuitry that selects a group of chained processing units.

We are thus unable to point to concrete evidence in this record in support of the examiner's findings. Cf In re Zurko, 258 F.3d 1379, 1386, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001) (in a determination of unpatentability "the Board must point to some concrete evidence in the record in support of...[the]...findings"). We do not sustain the rejection of claims 1-3 and 9-11.

CONCLUSION

The rejection of claims 1-3 and 9-11 under 35 U.S.C. § 103 as being unpatentable over Lesthievent is reversed.

REVERSED

KENNETH W. HAIRSTON
Administrative Patent Judge

ANITA PELLMAN GROSS
Administrative Patent Judge

HOWARD B. BLANKENSHIP
Administrative Patent Judge

) BOARD OF PATENT APPEALS AND INTERFERENCES

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